

### 128K x 8 Static RAM

#### Features

- **Low voltage range:**
  - 2.7V–3.6V (CY62128V)
  - 2.3V–2.7V (CY62128V25)
  - 1.6V–2.0V (CY62128V18)
- **Low active power and standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

#### Functional Description

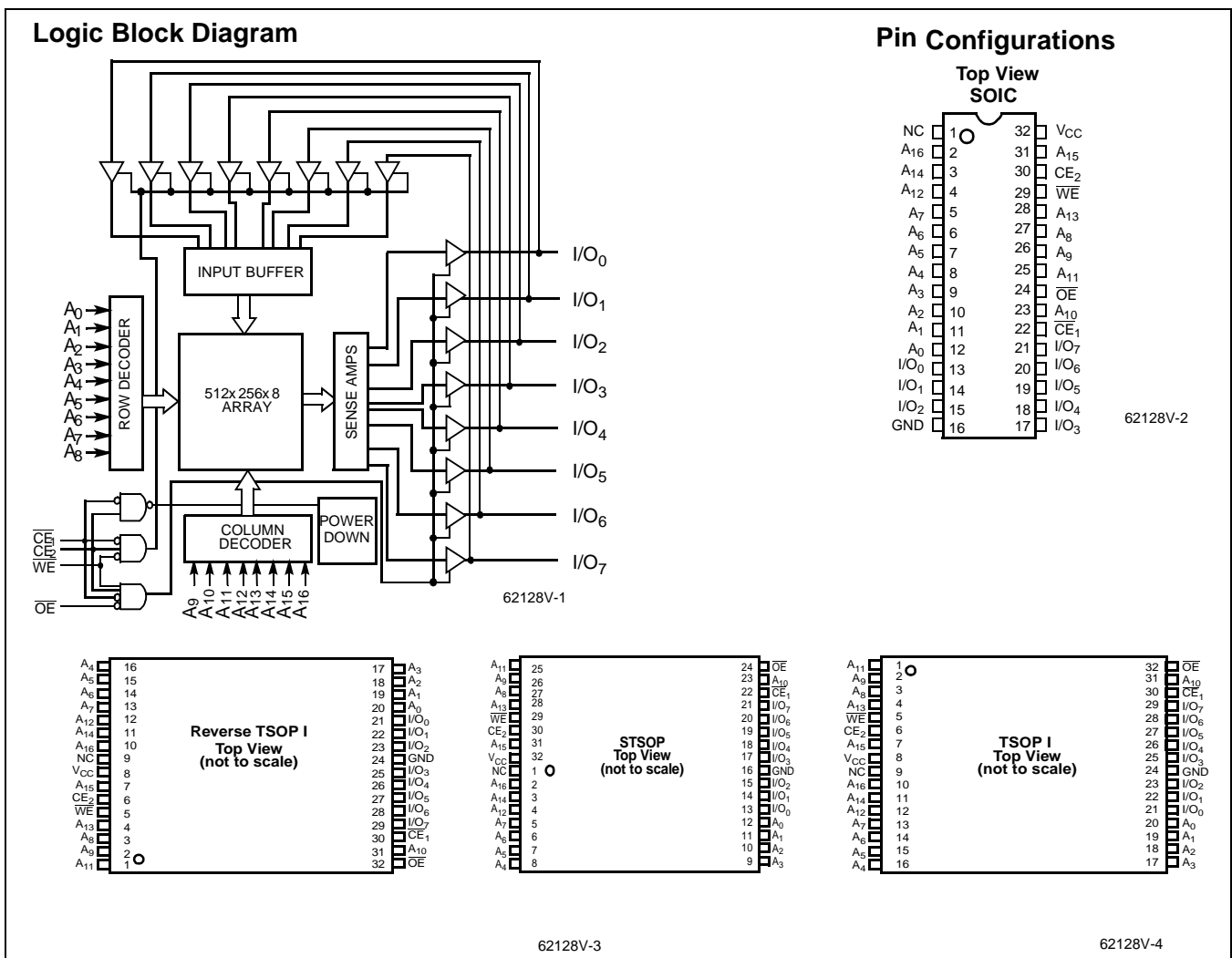
The CY62128V family is composed of three high-performance CMOS static RAMs organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $CE_2$ ), an active

LOW Output Enable ( $\overline{OE}$ ) and three-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected. The CY62128V family is available in the standard 450-mil-wide SOIC, 32-lead TSOP-I, and STSOP packages.

Writing to the device is accomplished by taking Chip Enable one ( $\overline{CE}_1$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW and the Chip Enable two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable one ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) and Chip Enable two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... -0.5V to +4.6V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Output Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	1.6V to 3.6V
Industrial	-40°C to +85°C	1.6V to 3.6V

**Product Portfolio**

Product	V <sub>CC</sub> Range			Speed	Power Dissipation (Commercial)			
	Min.	Typ. <sup>[2]</sup>	Max.		Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
					Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
CY62128V	2.7V	3.0V	3.6V	55, 70 ns	20 mA	40 mA	0.4 μA	100 μA (XL = 10 μA)
CY62128V25	2.3V	2.5V	2.7V	100 ns	15 mA	20 mA	0.3 μA	50 μA (LL = 12 μA)
CY62128V18	1.6V	1.8V	2.0V	200 ns	10 mA	15 mA	0.3 μA	30 μA (LL = 10 μA)

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62128V-55/70			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	2.4			V	
V <sub>OL</sub>	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$			0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2		$V_{CC} + 0.5V$	V	
V <sub>IL</sub>	Input LOW Voltage		-0.5		0.8	V	
I <sub>IX</sub>	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	±1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1	±1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	Com'l, 70 ns	L	20	40	mA
				LL, XL	20	40	
			Ind'l, 55 ns	LL	23	50	
				Ind'l, 70 ns	L	20	
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	Com'l, 70 ns	L	15	300	μA
				LL, XL	15	300	
			Com'l, 55 ns	LL	17	350	
				Ind'l	L	15	
LL	15	300					

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC \text{ Typ.}}, T_A = 25^\circ\text{C}$ .

**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions	CY62128V-55/70			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.		
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	L	0.4	100	μA
				LL		15	μA
				XL		10	μA
			Ind'l	L	0.4	100	μA
				LL		30	μA

**Electrical Characteristics** Over the Operating Range

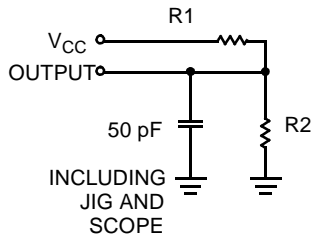
Parameter	Description	Test Conditions	CY62128V25-100			CY62128V18-200			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -0.1 mA	2.4			0.8* V <sub>CC</sub>			V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 0.1 mA			0.4			0.2	V	
V <sub>IH</sub>	Input HIGH Voltage		2		V <sub>CC</sub> +0.5	0.7* V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	
V <sub>IL</sub>	Input LOW Voltage		-0.5		0.8	-0.5		0.3* V <sub>CC</sub>	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	±1	+1	-1	±0.1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	±1	+1	-1	±0.1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	L		15	20		10	15	mA
			LL							
I <sub>SB1</sub>	Automatic CE Power-Down Current— TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	L		15	300		5	100	μA
			LL							
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	L		0.4	50		0.4	30	μA
			LL			12			10	μA
		Indust'l Temp Range	LL			24			20	μA

**Capacitance<sup>[3]</sup>**

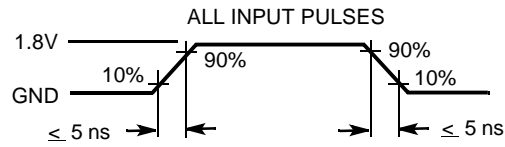
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.0V	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

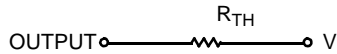
**AC Test Loads and Waveforms**


62128V-5



62128V-6

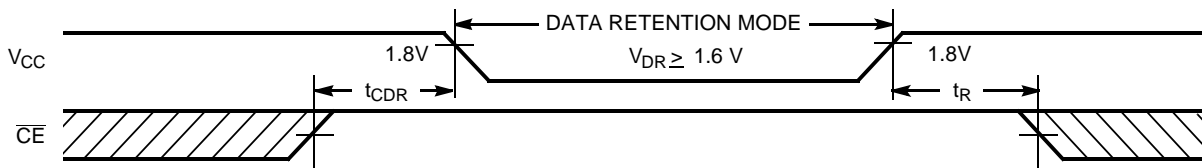
Equivalent to: THÉVENIN EQUIVALENT



Parameters	3.3V	2.5V	1.8V	Unit
R1	1213	15909	10800	Ohms
R2	1378	4487	4154	Ohms
$R_{TH}$	645	3500	3000	Ohms
$V_{TH}$	1.75V	0.55V	0.50V	Volts

**Data Retention Characteristics (Over the Operating Range)**

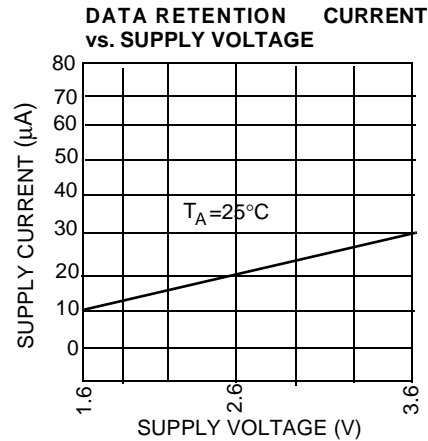
Parameter	Description	Conditions <sup>[4]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit	
$V_{DR}$	$V_{CC}$ for Data Retention		1.6			V	
$I_{CCDR}$	Data Retention Current	Com'l	L	$V_{CC} = 2V$ $CE \ge V_{CC} - 0.3V$ , $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$ No input may exceed $V_{CC} + 0.3V$	0.4	10	$\mu A$
			LL, XL			10	$\mu A$
		Ind'l	L			20	$\mu A$
			LL			20	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns	
$t_R$	Operation Recovery Time		$t_{RC}$			ns	

**Data Retention Waveform**


C62128V-7

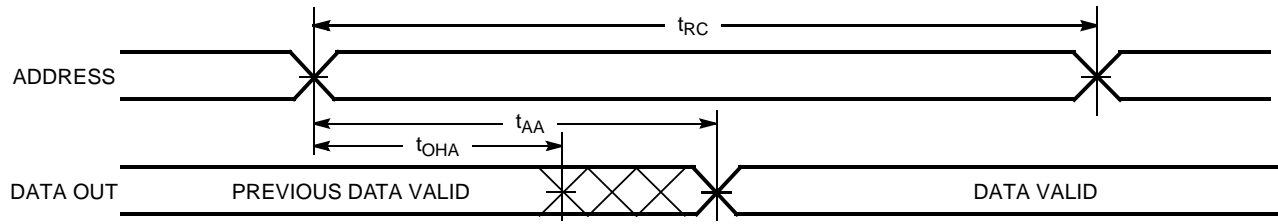
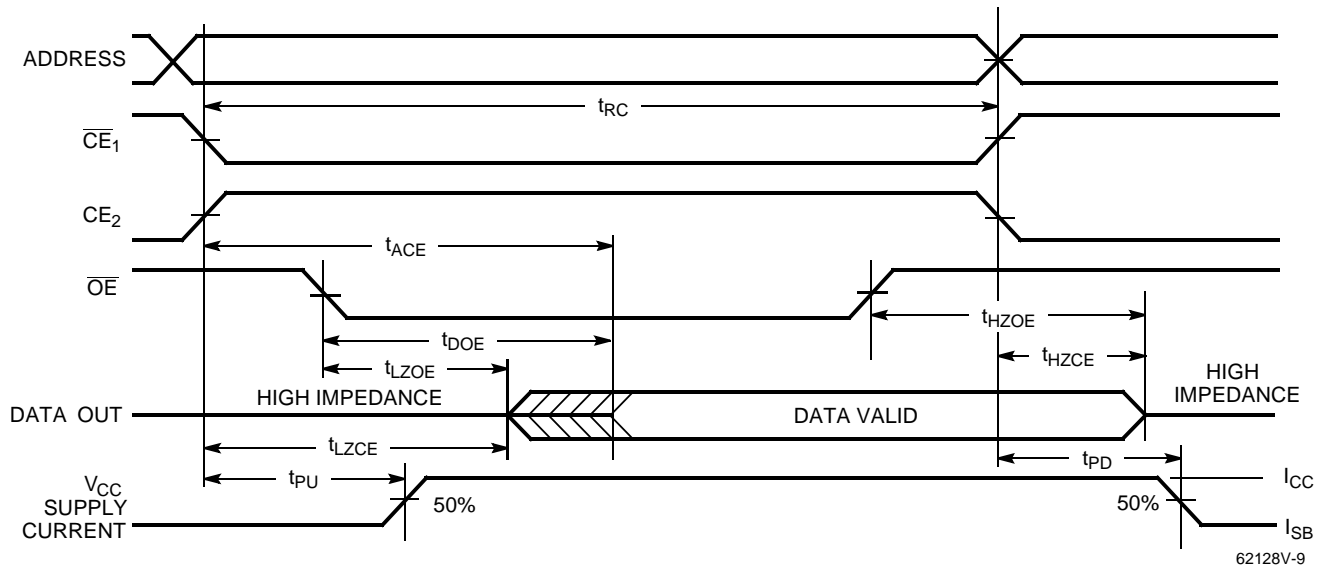
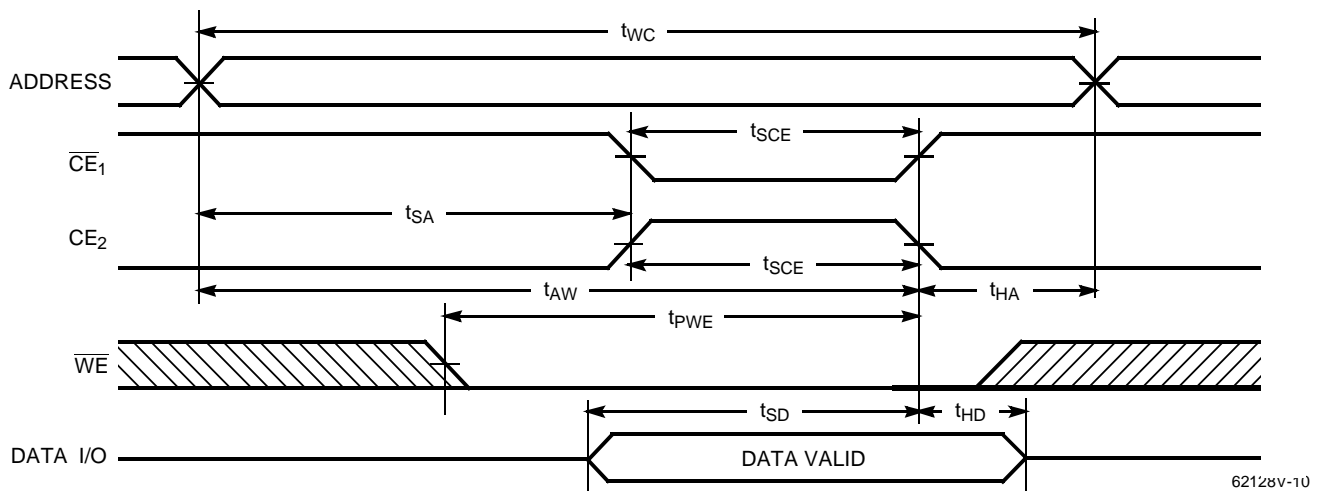
**Note:**

- No input may exceed  $V_{CC} + 0.3V$ .

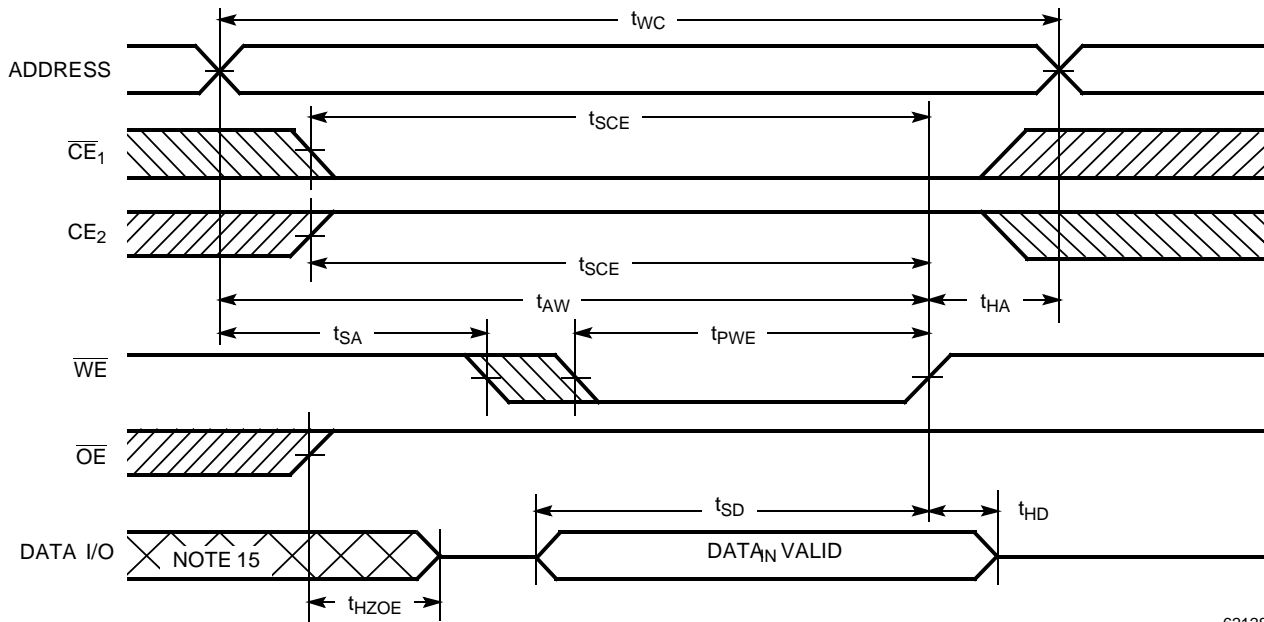
**Data Retention Current Graph** (for "L" version only)

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

Parameter	Description	62128V-55		62128V-70		62128V25-100		62128V18-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	55		70		100		200		ns
t <sub>AA</sub>	Address to Data Valid		55		70		100		200	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		10		10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70		100		200	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		20		35		75		125	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	10		10		10		10		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		20		25		50		75	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	10		10		10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		20		25		50		75	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		55		70		100		200	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	55		70		100		200		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		100		190		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		100		190		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	45		55		90		125		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		30		60		100		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		20		25		50		100	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	5		5		10		15		ns

- Test conditions assume signal transition time of 5 ns or less timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CE<sub>1</sub> LOW, CE<sub>2</sub> HIGH, and WE LOW. CE<sub>1</sub> and WE signals must be LOW and CE<sub>2</sub> HIGH to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Waveforms**
**Read Cycle No. 1<sup>[10, 11]</sup>**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11, 12]</sup>**

**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[13, 14]</sup>**

**Notes:**

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13, 14]</sup>**


62128V-11

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Note:**

15. During this period, the I/Os are in output state and input signals should not be applied.

**Ordering Information**

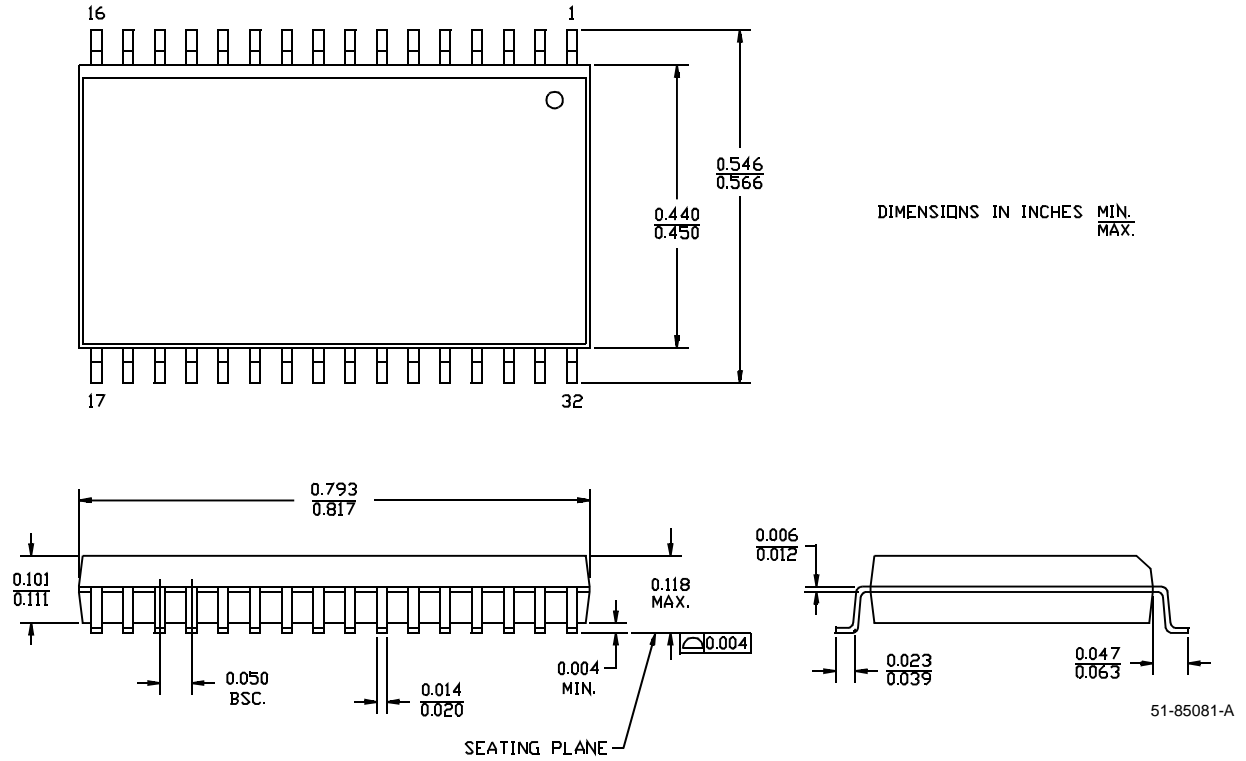
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range	
55	CY62128VLL-55ZAI	ZA32	32-Lead STSOP Type 1	Industrial	
70	CY62128VL-70SC	S34	32-Lead 450-Mil SOIC	Commercial	
	CY62128VLL-70SC				
	CY62128VL-70ZC	Z32	32-Lead TSOP Type 1		
	CY62128VLL-70ZC				
	CY62128VL-70ZAC	ZA32	32-Lead STSOP Type 1		
	CY62128VLL-70ZAC				
	CY62128VLL-70ZRC	ZR32	32-Lead Reverse TSOP Type 1		
	CY62128VLL-70SI	S34	32-Lead 450-Mil SOIC		Industrial
	CY62128VL-70ZI				
	CY62128VLL-70ZI	Z32	32-Lead TSOP Type 1		
	CY62128VL-70ZAI				
	CY62128VLL-70ZAI	ZA32	32-Lead STSOP Type 1		
CY62128VLL-70ZRI					
200	CY62128V18L-200ZC	Z32	32-Lead TSOP Type 1	Commercial	
	CY62128V18L-200ZAI	ZA32	32-Lead STSOP Type 1	Industrial	
	CY62128V18LL-200ZAI				

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Package Diagrams

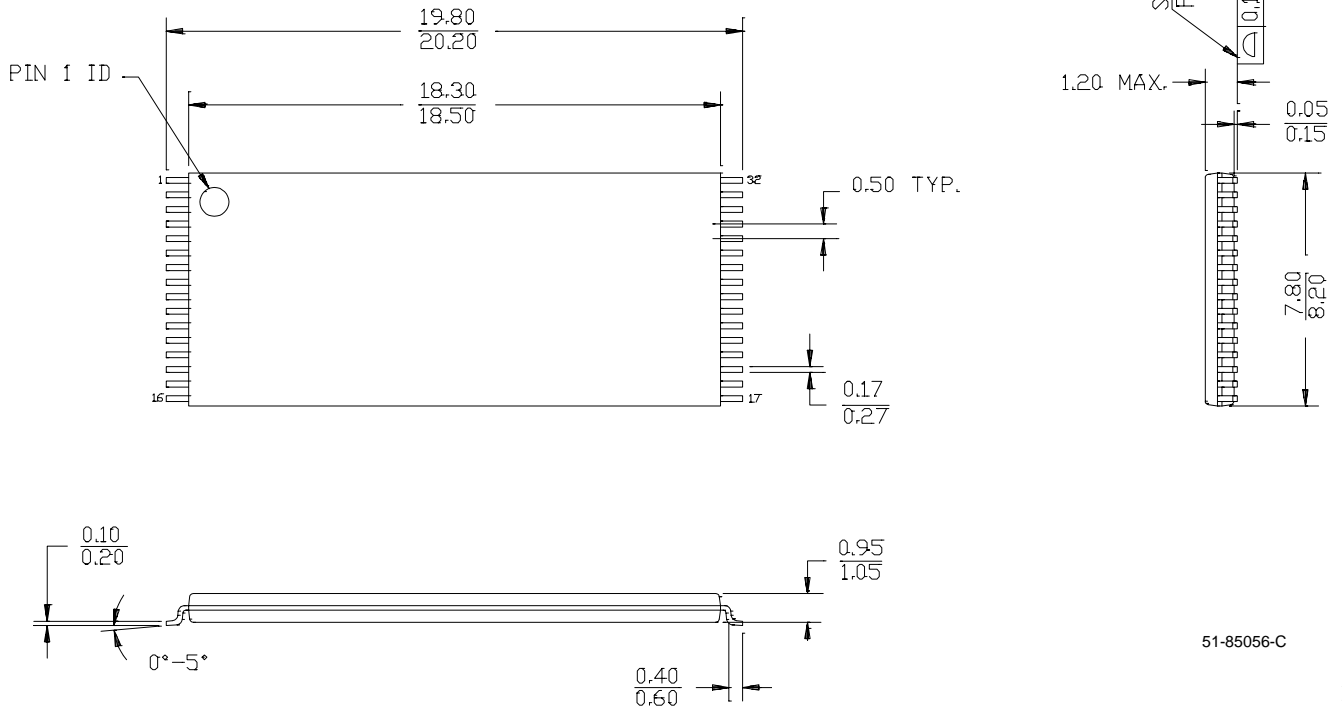
32-Lead (450 MIL) Molded SOIC S34



Package Diagrams

32-Lead Thin Small Outline Package Z32

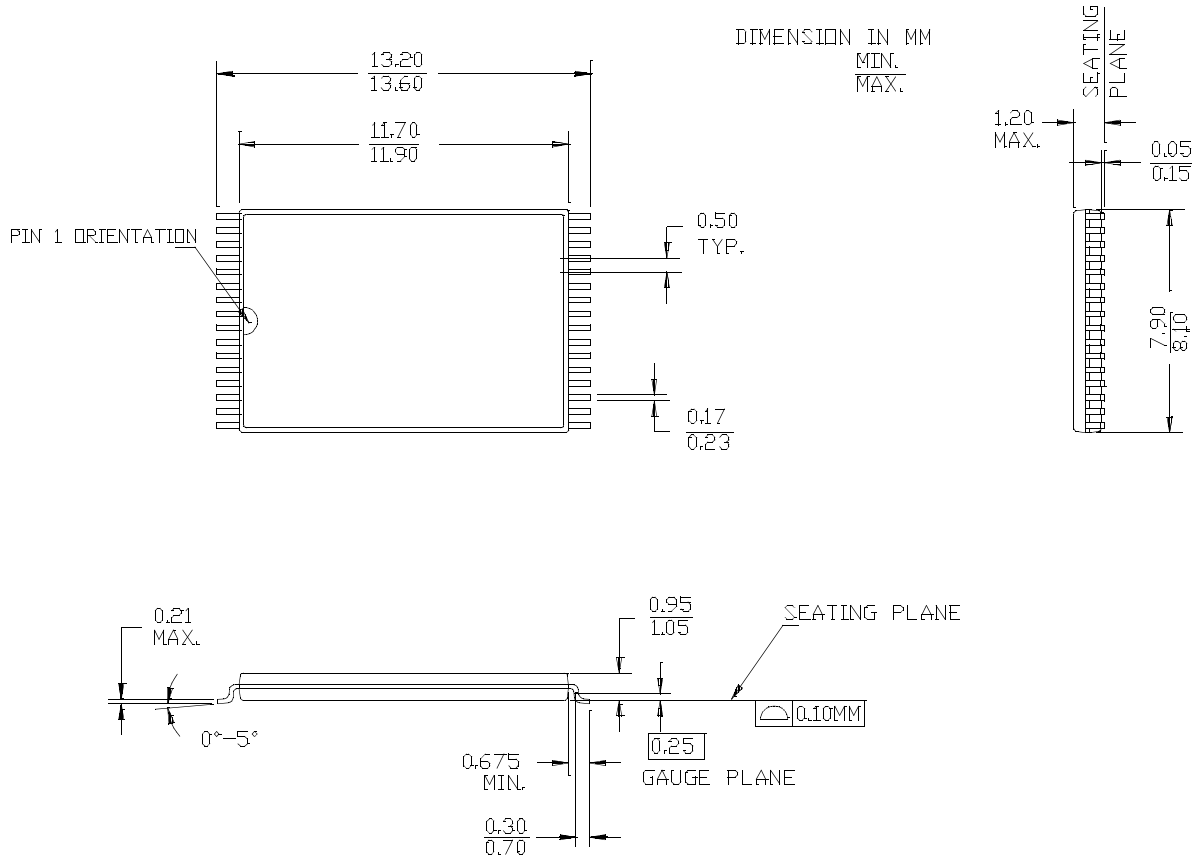
DIMENSION IN MM  
MIN.  
MAX.



51-85056-C

Package Diagrams

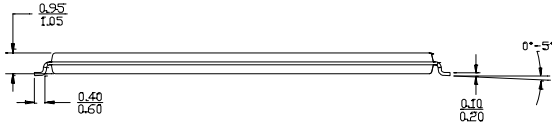
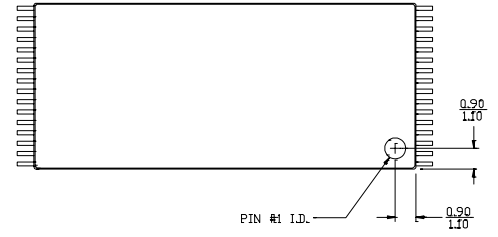
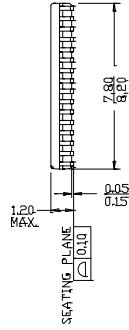
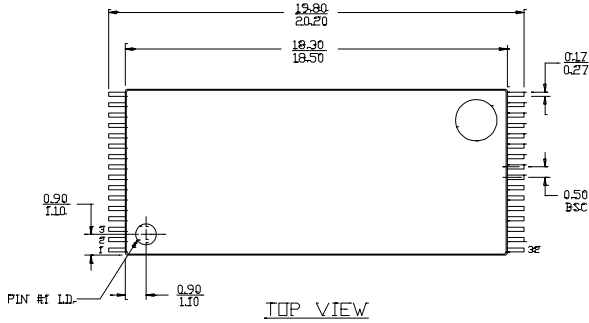
32-Lead Shrunk Thin Small Outline Package ZA32



51-85094-C

Package Diagrams

32-Lead Reverse Thin Small Outline Package ZR32



DIMENSION IN MM  
MIN.  
MAX.

51-85089-B